REMARKS

STATUS OF THE CLAIMS

Claims 1-16 are pending in the application.

A substitute specification in proper idiomatic English and in compliance with 37 CFR 1.52(a) and (b) is required. Also, the specification is objected to under the first paragraph of 35 USC 112.

Claim 1 is objected to due to informalities. Claim 1 is amended taking into consideration the Examiner's comments.

Claims 1, 4, 7 and 14-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite.

Claims 1-3 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli et al. (US Patent No. 6,374,330) in view of Bourekas et al. (U.S. Patent No. 6,128,703).

Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli in view of Bourekas and further in view of Prudvi et al. (U.S. Patent No. 6,378,048).

Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli in view of Bourekas and further in view of Gornish et al. (U.S. Patent No. 5,752,037).

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli in view of Bourekas, further in view of Gornish as applied to claims 11 and 12, and further in view of Steely, Jr. et al. (U.S. Patent No. 5,966,737).

Claims 1, 4, 7, 14-16 are amended. Thus, claims 1-16 remain pending for reconsideration, which is respectfully requested.

No new matter has been added in this Amendment. The rejections are hereby traversed.

SPECIFICATION

The Examiner requests a substitute specification in proper idiomatic English and in compliance with 37 CFR 1.52(a) and (b).

37 CFR 1.125(a) provides that a substitute specification might be required "[i]f the

number or nature of the amendments or the legibility of the application papers renders it difficult to consider the application ...." However, upon a review of the specification, and in view of the Office Action not specifying why the specification has faulty English and/or not specifying any typographical errors, the Applicant respectfully asserts that the specification uses proper idiomatic English sentences and the specification is not difficult to consider. In particular, the specification has been reviewed, and in the previous Amendment, the specification was amended to correct a few minor typographical errors. Further, a substitute specification has been previously filed in the present Application on February 13, 2004 in response to the Office Action mailed November 14, 2003, taking into consideration Examiner comments. Therefore, the specification is not difficult to consider, and the English sentences are in proper idiomatic English. Therefore, a second substitute specification requirement is not appropriate, and withdrawal of the objection in view of the remarks and the specification amendments is respectfully requested.

Regarding the 35 USC 112, first paragraph, objection to the specification, in page 2, item 3, of the Office Action, the Applicant, including inventor, has considered the application, taking into consideration Examiner comments, and respectfully assert that the specification "contains a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention," which also becomes more apparent in view of the claim amendments and remarks herein concerning patentably distinguishing differences between the claimed present invention and the relied upon references. Therefore, withdrawal of the 35 USC 112, first paragraph, objection is respectfully requested.

Further, according to the foregoing, paragraph 64, line 10 is corrected by being amended to be consistent with the previous sentence in paragraph 64.

CLAIM REJECTION – 35 USC 112, SECOND PARAGRAPH

Independent claims 1, 4, 7 and 14-16 are rejected under 35 USC 112, second paragraph, for indefiniteness. Independent claims 1, 4, 7 and 14-16 are amended, taking into consideration Examiner comments. Withdrawal of the indefiniteness rejection is respectfully requested.

CLAIM REJECTIONS – 35 USC 103

The independent claims are 1, 4, 7 and 14-16.

The Office Action maintains, from the previous Office Action, the rejection of claims 1-16 over Arimilli, Bourekas, Prudvi, Gornish, and Steely. In particular, independent claims 1, 4, 7 and 14-16 are rejected over a combination of Arimilli and Bourekas.

INDEPENDENT CLAIMS 1 AND 14

Against the previous rejection rationale that claim 1 is obvious over Arimilli and Bourekas, arguments were presented in the previous Amendment that Bourekas discloses a single cache whereas the claimed present invention sets forth, unlike Bourekas, a "***a weak read operation that fails a pre-fetch request*** following a read request from one of the processors, ~~in a case that~~***if*** at a time of generation of ~~a~~the pre-fetch request, ***the state tags of other cache devices must be changed to read*** ~~***following a read request from one of the processors***~~ ***the data stored in the other cache devices***" (e.g., claims 1, 14), thereby the claimed present invention being directed to a plurality of caches. But the Office Action still maintains rejection of claim 1 as being obvious over Arimilli and Bourekas. The Office Action Response to Arguments is described in pages 12-13, item 11.

In other words, because Bourekas discloses a single cache, there is no motivation to be combined with Arimilli. Even if one combined Arimilli and Bourekas, the combined system would not yield the claimed present invention's, "***a weak read operation that fails a pre-fetch request following a read request from one of the processors, ~~in a case that~~if at a time of generation of ~~a~~the pre-fetch request, the state tags of other cache devices must be changed to read ~~following a read request from one of the processors~~ the data stored in the other cache devices***" (e.g., claims 1, 14). The rejection rationale acknowledges that Arimilli does not disclose the claimed present invention's, "***a weak read operation that fails a pre-fetch request following a read request from one of the processors***," so the rejection relies on Bourekas. Regarding Bourekas, it will be clarified in details that Bourekas has no description about the claimed present invention's "***a weak read operation that fails a pre-fetch request following a read request from one of the processors***," as follows. The basic operation of prefetch processing in Bourekas is shown in the flowchart of FIG. 5, to do nothing and cause an end of prefetch (not a failure) in a cache hit (column 8, lines 6-15). In a cache mishit, the data is stored in cache from the main memory to complete prefetch. Also in the

case of a cache mishit, at operation 506, prefetch is brought to an end upon occurrence of an exception, such as a parity error or a bus error, as a matter of course.

The rejection rationale in Response to Arguments on pages 12-13, item 11 specifically relies on a description of the processing blocks 806 to 812 in the flowchart shown in FIG. 8 of Bourekas. However, Bourekas' FIG. 8, operations 806-812, relate to Bourekas' prefetch instruction containing an ignore hit indicator. Bourekas in column 5, lines 18-22, discloses:

> Within the prefetch instruction is an ignore hit indicator that provides an indication to the primary cache as to whether the specified data should be retrieved from the main memory, even if the specified data is stored within the primary cache.

More particularly, for this portion of Bourekas' FIG. 8 flowchart, when, at operation 804, a condition of ignoring the cache hit is determined, and, at operation 805, the data of the fetch address indicates a cache hit, at operation 810, the state is brought into an invalid state after operation 808 writing back into the main memory in the modified state. At operation 806, in conditions other than the modified state, at operation 810, the state is brought into the invalid state without writing back. Thereafter, if the state is not exceptional, the process advances to operation 814, in which the state at the fetch address from the main memory is stored in the cache, thus completing prefetch. Therefore, in Bourekas, even when the prefetch data exist on the cache, data is retrieved from the main memory after totally invalidating (operation 810). For the modified state (operation 806), since the data on the cache are the latest and the data on the main memory are old, the only fact is that the data on the cache are written back to the main memory (operation 808, column 10, lines 14-22, which is relied upon in the rejection) and then prefetched from the main memory. Also, in Bourekas, when, at operation 805, prefetched data is non-existent on the cache, i.e., in the case of a mishit, at operation 812, upon occurrence of an exception, such as a parity error or a bus error, at operation 818 prefetch is terminated. Further, in Bourekas, at operation 810, the cache line is invalidated and, at operation 814, the prefetch is completed, which differs than the claimed present invention's, "***a weak read operation that fails a pre-fetch request following a read request from one of the processors, ~~in a case that~~if at a time of generation of ~~a~~the pre-fetch request, the state tags of other cache devices must be changed to read ~~following a read request from one of the processors~~ the data stored in the other cache devices***" (e.g., claims 1 and 14). In other words, Bourekas' invalidation (810) and prefetch completion from main memory (814) in case the ignore hit indicator has been set in operation 804, differs from the claimed present

invention's ***causing a failure of a prefetch request***. In Bourekas, the only an abnormal end of a prefetch request is caused at operation 812 by a hardware error, which is also not the same as the claimed present invention's "***a weak read operation that fails a pre-fetch request following a read request from one of the processors, ~~in a case that~~if at a time of generation of ~~a~~the pre-fetch request, the state tags of other cache devices must be changed to read ~~following a read request from one of the processors~~ the data stored in the other cache devices***" (e.g., claims 1 and 14).

Since Bourekas discloses or suggests nothing positively about ***causing failure*** of a prefetch request, a combination of Bourekas with the cache device of multi-processor of Arimilli could not lead to failure of a prefetch request when it is necessary to change the state of other cache devices. What is derived from the application of processing of a prefetch request in Bourekas' cache device to an Arimilli multi-cache device is that, upon occurrence of a prefetch request, the prefetch request is naturally brought to success by changing the state of the other cache devices, if data stored in other cache devices cannot be read unless the state tag thereof is changed. This is the very conventional art itself as stated in the present application. Accordingly, a combination of Bourekas and Arimilli fails to disclose or suggest the claimed present invention's, "a cache controller ~~for carrying out~~performing, as a pre-fetch protocol, ***a weak read operation that fails a pre-fetch request following a read request from one of the processors, ~~in a case that~~if at a time of generation of ~~a~~the pre-fetch request, the state tags of other cache devices must be changed to read ~~following a read request from one of the processors~~ the data stored in the other cache devices*** ~~must be read by changing state tags of the other cache devices, weak read operation for causing failure in said pre-fetch request as a pre-fetch protocol~~ (e.g., claims 1, 14). In other words, as recited in dependent claim 2, in contrast to a combined Bourekas and Arimilli, the claimed present invention provides,

> 2. (ORIGINAL) The cache device according to claim 1, wherein said cache memory distinguishes the stored data by a data-modified state (M), an exclusive state (E), a data-shared state (S) and an invalid state (I), each of which indicates validity of the state tag, and
>
> said cache controller ***causes failure in said pre-fetch request when the data corresponding to the pre-fetch request stored in the other cache devices is in the data-modified state (M) or the exclusive state (E)***.

Support for independent claims 1 and 14 can be found, for example, in FIG. 10, operations 4 and 5, and paragraph 56 of the substitute specification.

Further, the following is based upon inventor comments:

Inventor agrees with the above-mentioned comment on differences between Bourekas and the claimed present invention. Particularly, the rejection rationale seems to erroneously recognize the comparisons of Bourekas' Fig. 8. The terms "modified" and "hit" subjected to judgment in Bourekas' Fig. 8 relate to the state in the interior of the cache of the processor having issued a prefetch. In the present invention, on the other hand, what is to be judged for determining the prefetch action is the state in the caches of other processors than the processor issuing the prefetch. There is a confusion in the rejection rationale about this point: The Examiner has erroneously judged as if Bourekas' disclosure were based on similar judgment conditions.

The present invention relates to the action to be taken when a prefetch command is issued by the processor, and data corresponding to the address does not exist within its own cache. Referring to Bourekas' Fig. 8, the present invention relates to the "Completed Prefetch" described in block 814 [i.e., in the claimed present invention the prefetch is failed (additional explanation added herein)]. The present invention is perfectly independent of Bourekas. If the present invention is referred to as A, and Bourekas' invention, as B, an invention A+B having the features of the both inventions can be formed by combining these inventions. Between inventions A and B, there is no relationship of permitting derivation of invention A by analogy from Bourekas' invention B.

Accordingly, in contrast to Arimilli and Bourekas, the claimed present invention provides, "a cache controller ~~for carrying out~~performing, as a pre-fetch protocol, ***a weak read operation that fails a pre-fetch request following a read request from one of the processors,*** ~~***in a case that***~~***if at a time of generation of*** ~~***a***~~***the pre-fetch request, the state tags of other cache devices must be changed to read*** ~~***following a read request from one of the processors***~~ ***the data stored in the other cache devices*** ~~must be read by changing state tags of the other cache devices, weak read operation for causing failure in said pre-fetch request as a pre-fetch protocol~~ (e.g., claims 1, 14).

Allowance of independent claims 1 and 14 is respectfully requested.

INDEPENDENT CLAIMS 4 (15) AND 7 (16)

No substantial reason for rejection based upon prior art is presented for independent claims 4 and 7, therefore claims 4 and 7 are allowable, as follows.

In contrast to the relied upon references, the claimed present invention recited in independent claims 4 and 15, as amended for clarity, using claim 4 as an example, provides:

> 4. (CURRENTLY AMENDED) A cache device set up in each of processors, interconnected to other cache devices in other processors and connected to a main memory, which comprises:
>
> a cache memory wherein a part of data in the main memory is stored in one or more cache lines and a state tag ~~using~~used to manage data consistency is set up in each of the cache lines, and
>
> a cache controller in response to a pre-fetch request following a read request from one of the processors, ***reading data without changing state tags of other cache devices and storing the read data in the cache memory with setup of a weak state (W), if*** ~~***for carrying out a pre-fetch protocol that in a case that***~~ ***at a time of generation of athe pre-fetch request, the state tags of the other cache devices must be changed to read*** ~~following a read request from one of the processors~~the data stored in the other cache devices, ~~must be read by changing state tags of the other cache devices, the data is read without changing the state tag and stored in the cache memory with setup of a weak state W,~~ and ***invalidating the data stored in the cache memory in the weak state W at a time of synchronization operation of memory consistency to attain data-consistency by software*** ~~the data in the cache memory in said weak state (W) is wholly invalidated~~.

Support for claims 4 and 15 can be found, for example, in FIG. 12 and paragraph 59 of the substitute specification. A benefit of the claimed present invention recited in independent claims 4 and 15 is to force a synchronization without changing the state tags of the other cache devices (see, paragraph 59, page 40 of the substitute specification).

In contrast to the relied upon references, the claimed present invention recited in independent claims 7 and 16, as amended for clarity, using claim 7 as an example, provides:

> 7. (CURRENTLY AMENDED) A cache device set up in each of processors, interconnected to other cache devices in other processors and connected to a main memory, which comprises:
>
> a cache memory wherein a part of data in the main memory is stored in one or more cache lines and a state tag ~~using~~used to manage data consistency is set up in each of the cache lines, and
>
> a cache controller ~~for carrying out~~ controlling a pre-fetch protocol according to a process comprising:
>
> setting as ~~the~~a state tag, at ~~the~~a time of generation of a pre-fetch request following a read request from one of the processors, a passive preservation mode P to data pre-fetched from ~~the~~ other cache devices or from the main memory,
>
> storing the pre-fetched data in said cache memory,
>
> not informing the other cache devices of the preservation of the data in said cache memory, when ~~the~~ data ~~corresponding to~~for a read request from the other cache devices ~~is~~corresponds to the pre-fetch data to which said passive preservation mode P is set, ~~the other cache devices of the preservation of the corresponding data,~~ and
>
> invaliding the pre-fetched data in the cache memory, when according to the read request from the other cache devices, none of the other cache devices store the corresponding data, and preserving said pre-fetch data as it is, when according to the read request from the other cache devices, the other cache devices share the corresponding data.

Support for independent claims 7 and 16 can be found, for example, in FIG. 14 and paragraphs 60-65 of the substitute specification. A benefit of the claimed present invention recited in independent claims 7 and 16 is to treat pre-fetch data as speculative and invalidate it unless a HIT line (shared) is asserted.

In page 4 of the Office Action, the indefiniteness rejection for claims 7 and 16 provides,

> when a particular data is pre-fetched to a cache and since none of the other cache devices has the particular data, that particular data gets invalidated. In other words, every time the data is pre-fetched to any cache devices, it is invalidated since none of the other cache devices stores the same data. So there will not be a case that any other (second) cache device would have the same particular data stored in it during the pre-fetch in other (first) cache device.

The claimed present invention as amended provides, "***not informing*** the other cache devices of the preservation of the data in said cache memory, ***when ~~the data corresponding to~~for a read request from the other cache devices ~~is~~corresponds to the pre-fetch data to which said passive preservation mode P is set***, ~~the other cache devices of the preservation of the corresponding data,~~ and invaliding the pre-fetched data in the cache memory, ***when according to the read request from the other cache devices, none of the other cache devices store the corresponding data***, and ***preserving said pre-fetch data as it is, when according to the read request from the other cache devices, the other cache devices share the corresponding data***." Accordingly, in claims 7 and 16, the invalidation and the preservation are expressly tied to a read request from other cache devices, such that cache data in a preservation mode might get invalidated in response to another data read request for data that corresponds to the data in the preservation mode. Support can be found, for example, in paragraphs 64-65 of the substitute specification.

More particularly, the following description explains operation and benefit of the claimed present invention as recited in independent claims 7 and 16. Usually, when data is read in a state in which the other cache devices store data, the state becomes an S state. After the S state, data writing requires an invalidation operation of the other cache devices, requiring a considerable overhead. However, if none of the cache devices hold data, the data can be stored in the E state. Data writing in the E state does not require an invalidation operation. Assume, for example, a case where the other cache devices are exclusively those holding data in the claimed present invention's P state. In this case, the cache device from which data is read is in the S state, thus requiring an invalidation operation upon writing. However, the P state originally represents data read out for a pre-fetch of which the existence has no practical importance. Therefore only for this P state data, it would be useless to be forced to select the S state rather than the E state (i.e., the E state should be selected). In other words, when

comparing the overhead for an invalidation request upon selection of the S state with the demerits of throwing away the pre-fetch data, the latter provides favorable merits. Independent claims 7 and 16, therefore, set forth a concept in which, in case of a read request by a cache device, if another cache device holding same data, stores the same data only in the P state, the data in the P state is thrown away so that the data by the requesting cache device can be read and held in the E state.

Therefore, independent claims 4, 7 and 15-16 are allowable.

CONCLUSION

In view of the claim amendment and remarks, withdrawal of the rejection of pending claims and allowance of pending claims is respectfully requsted.

If there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

Respectfully submitted,
STAAS & HALSEY LLP

Date: 2/3/2005

By: _____
Mehdi D. Sheikerz
Registration No. 41,307

1201 New York Ave, N.W., Suite 700
Washington, D.C. 20005
Telephone: (202) 434-1500
Facsimile: (202) 434-1501